

FIG. 1

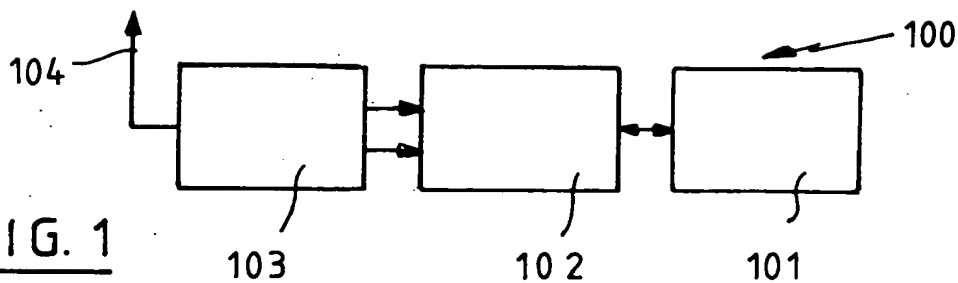
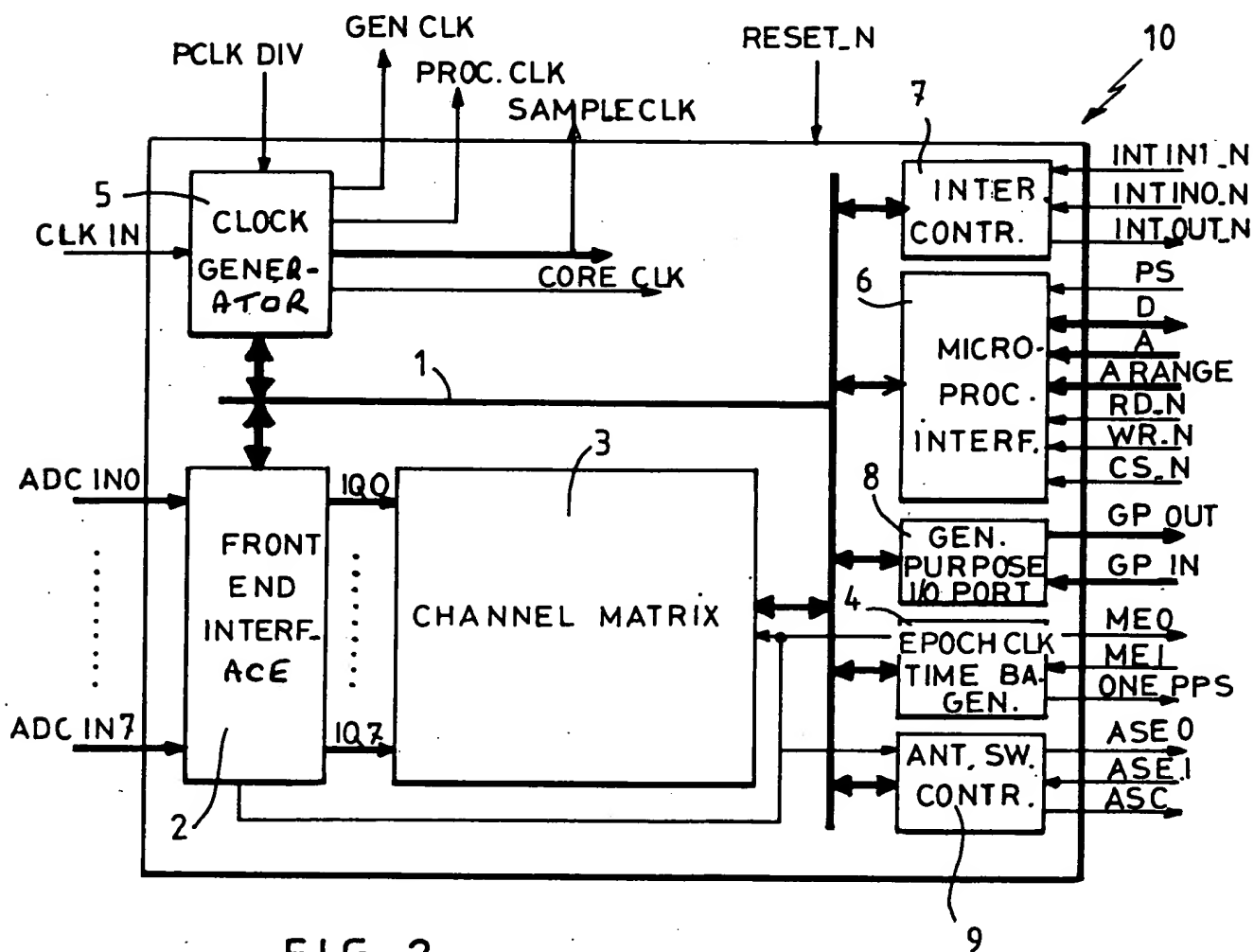


FIG. 2



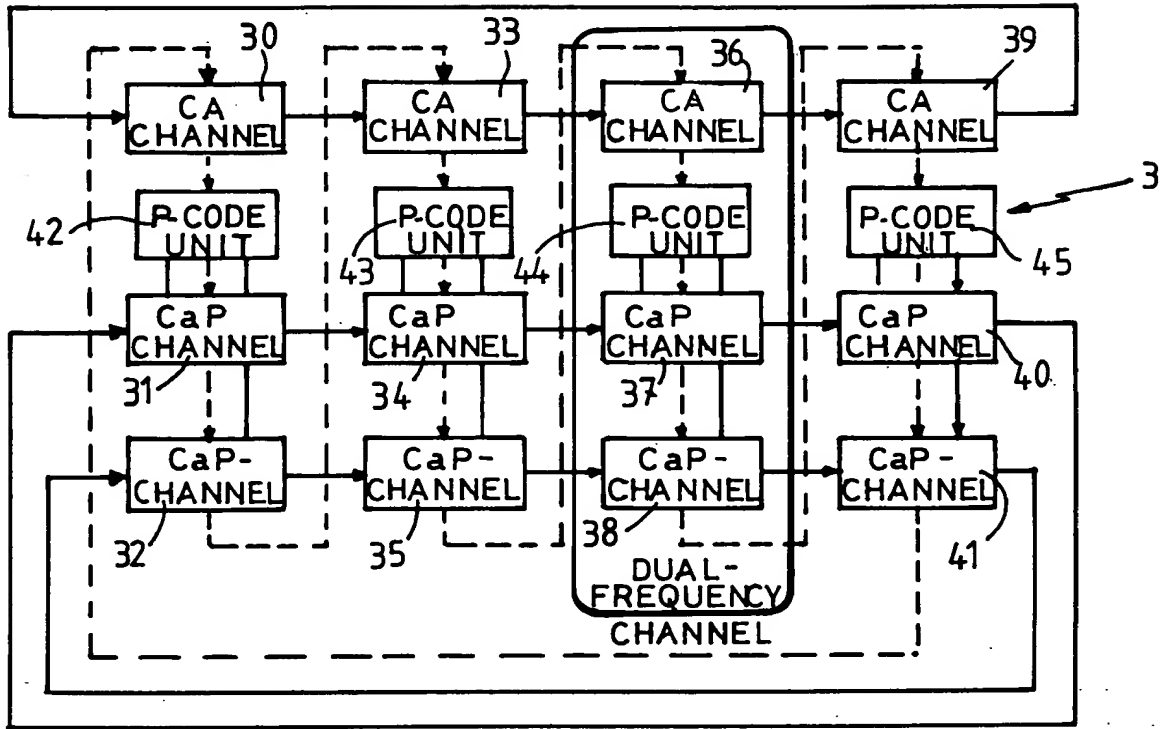


FIG. 3

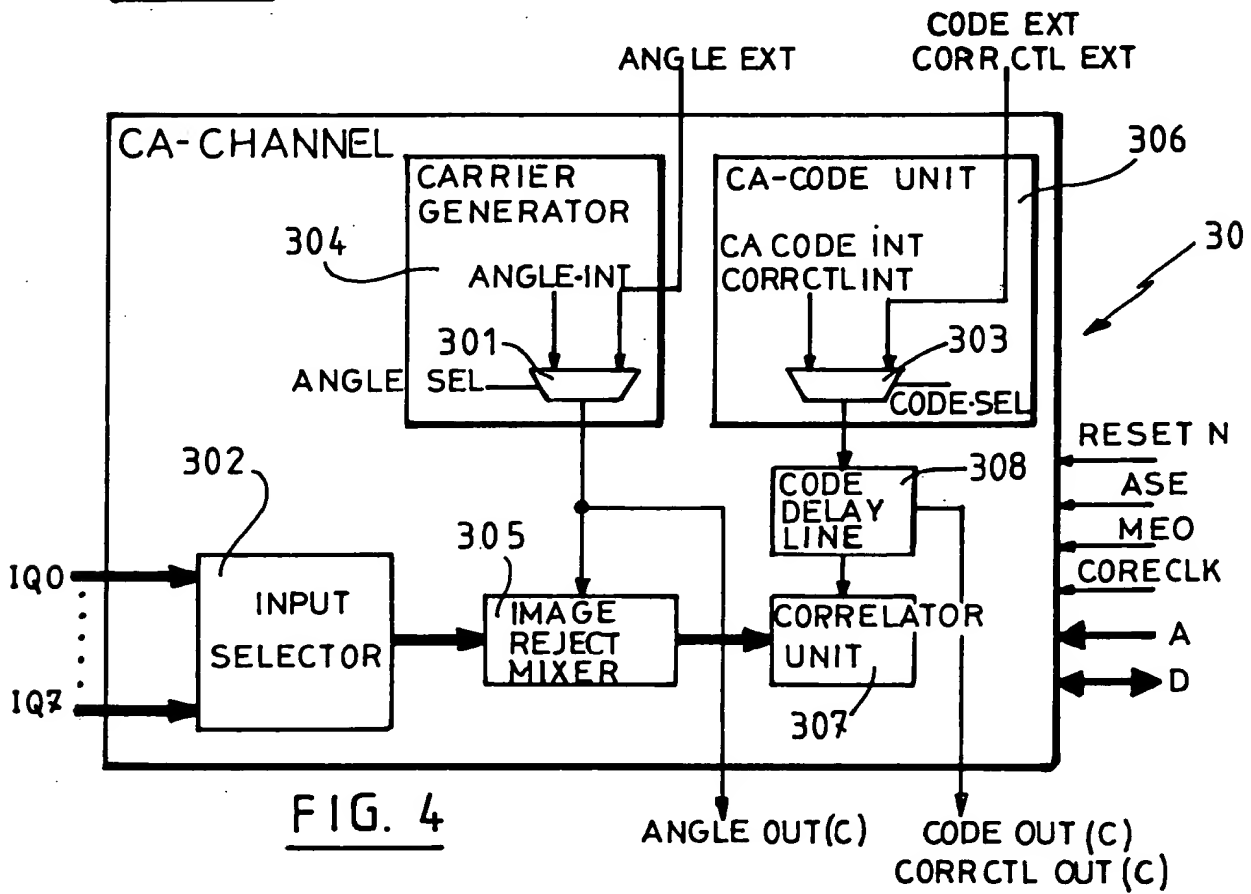


FIG. 4

FIG. 5

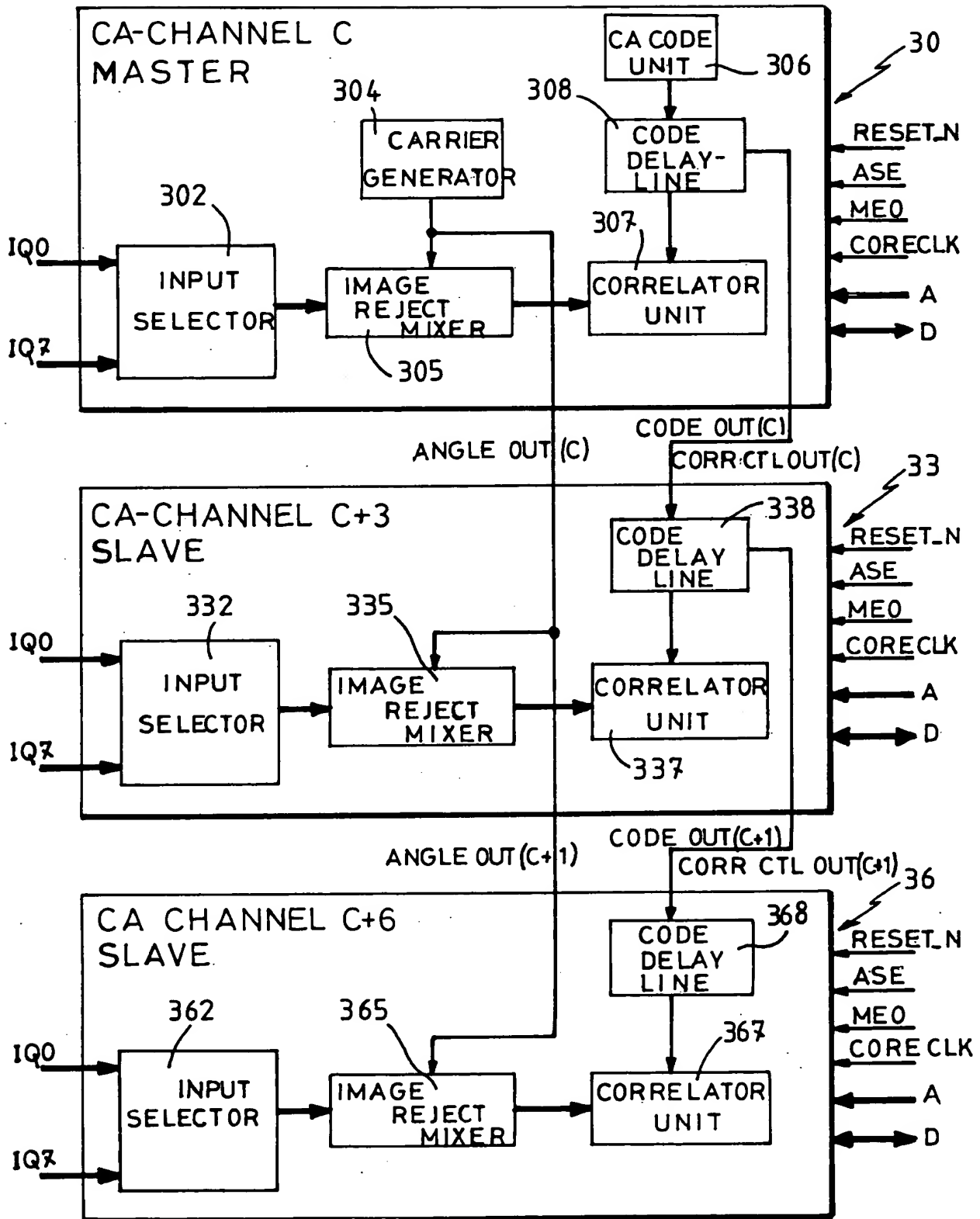
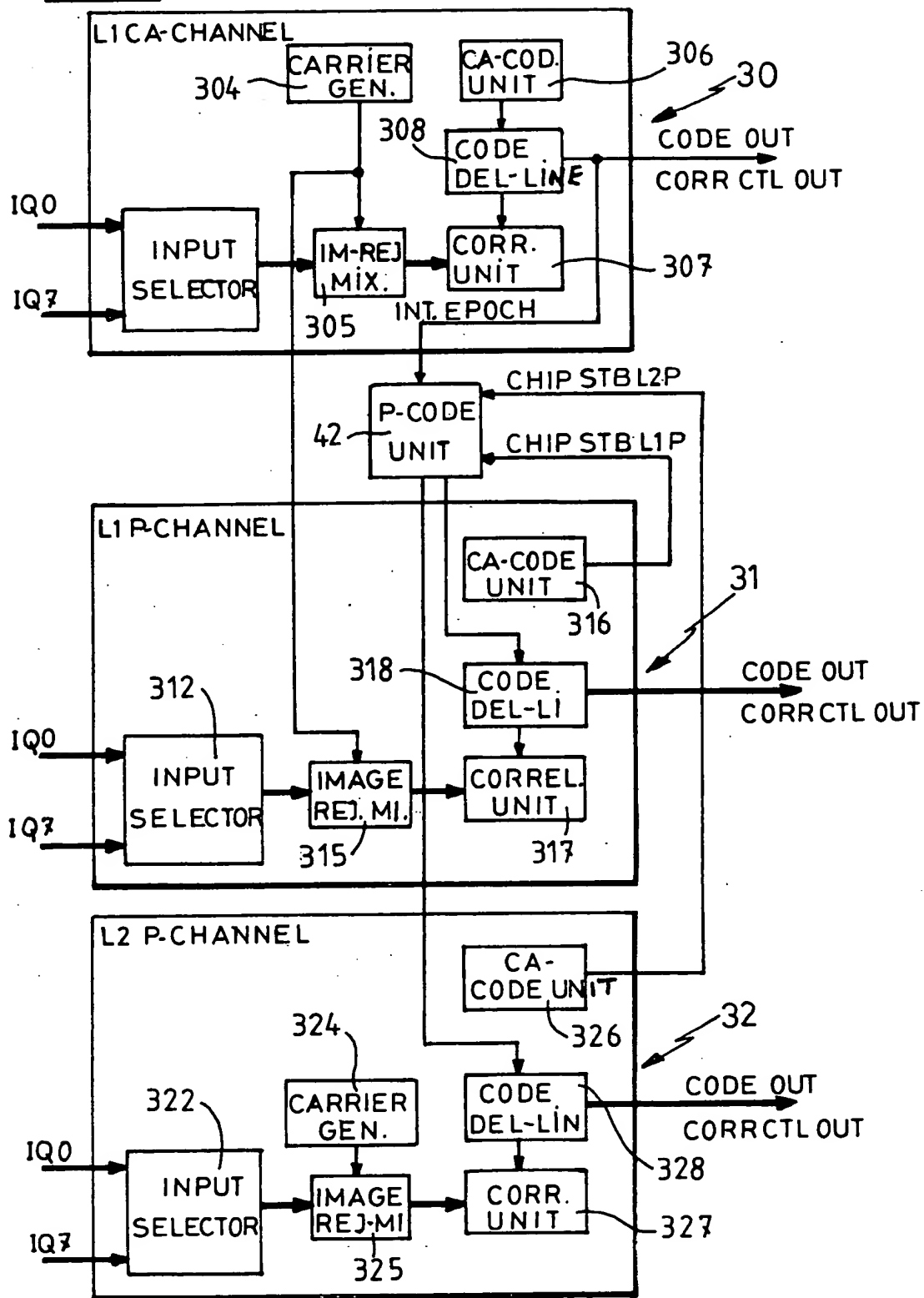


FIG. 6



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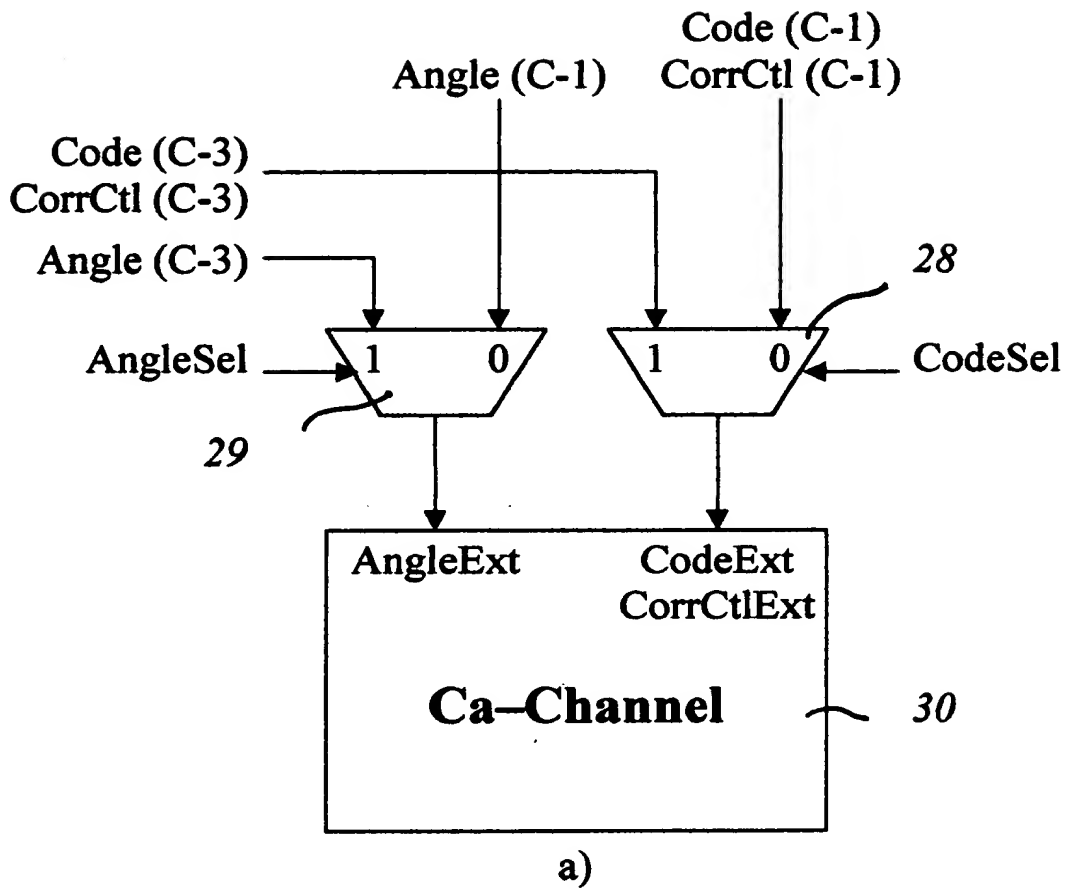
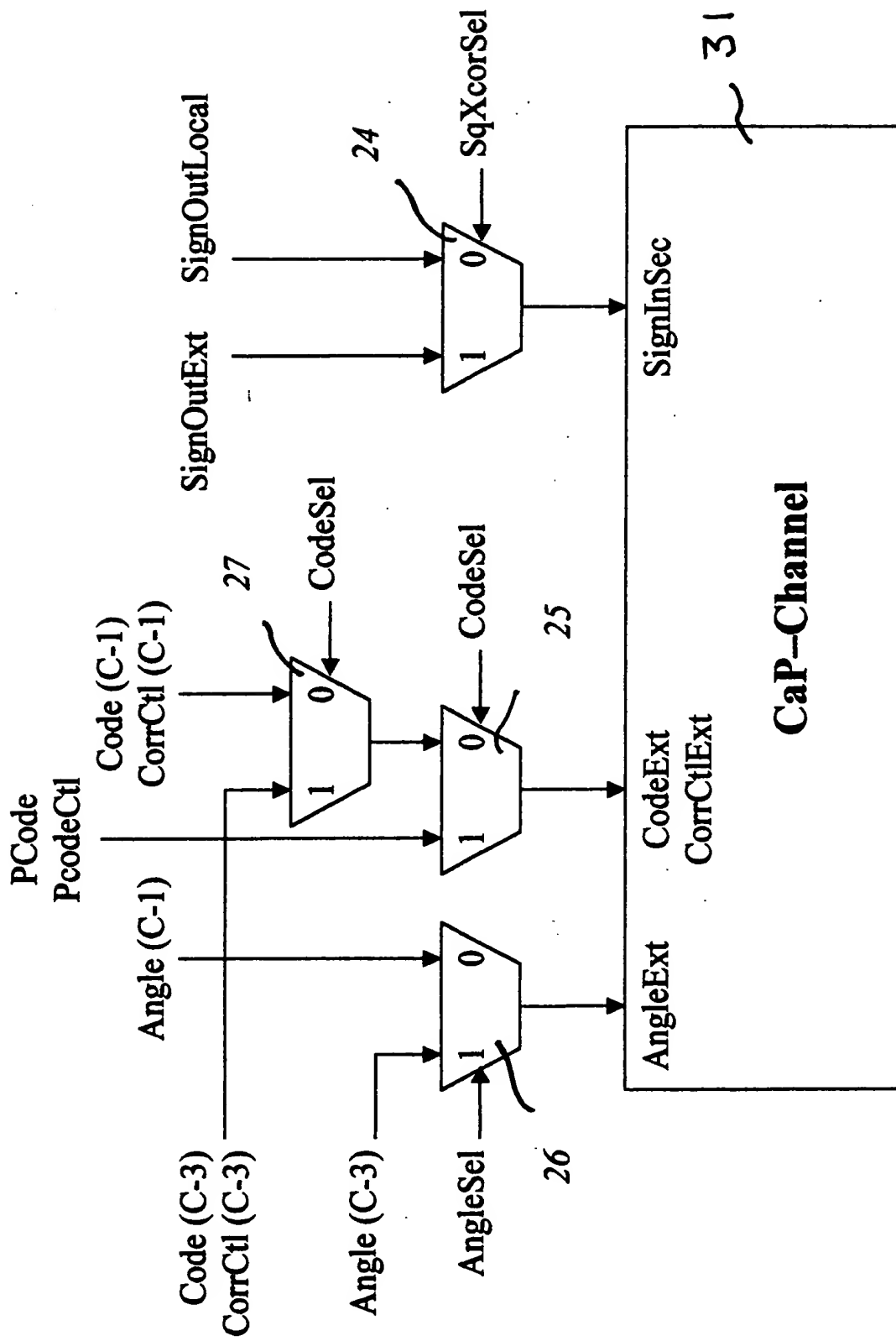


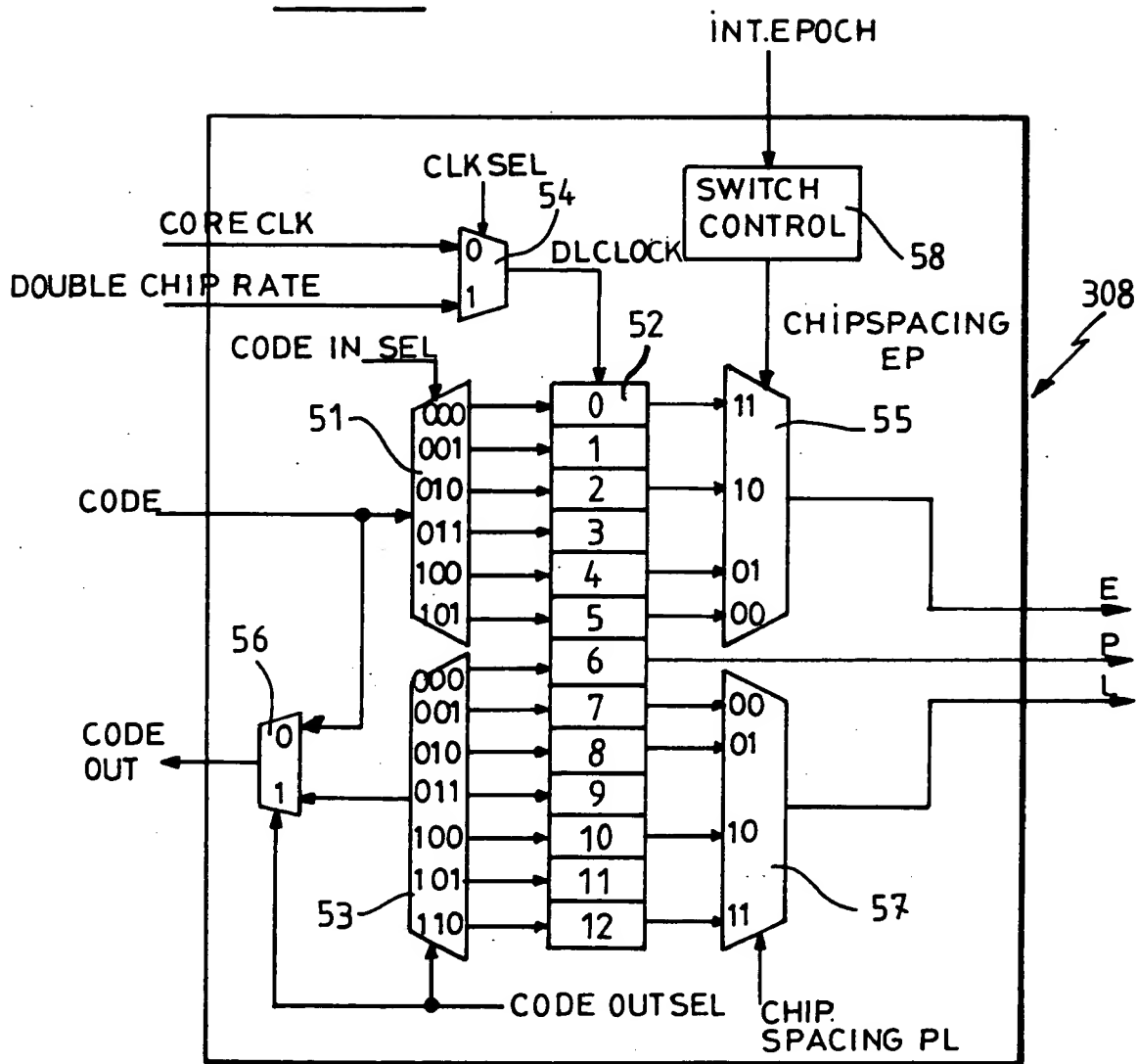
Fig. 7a

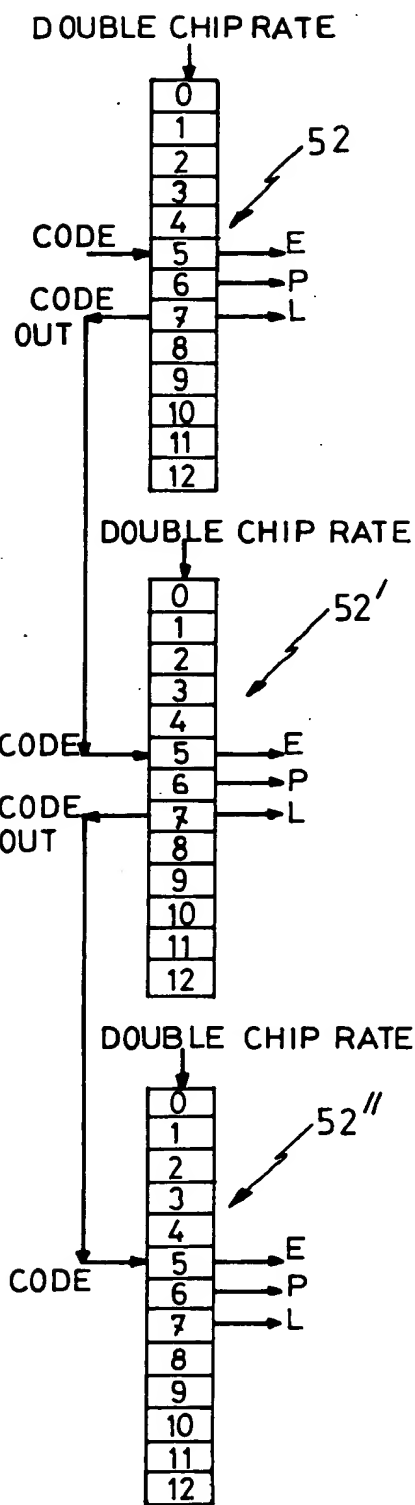


b)

Fig. 7b

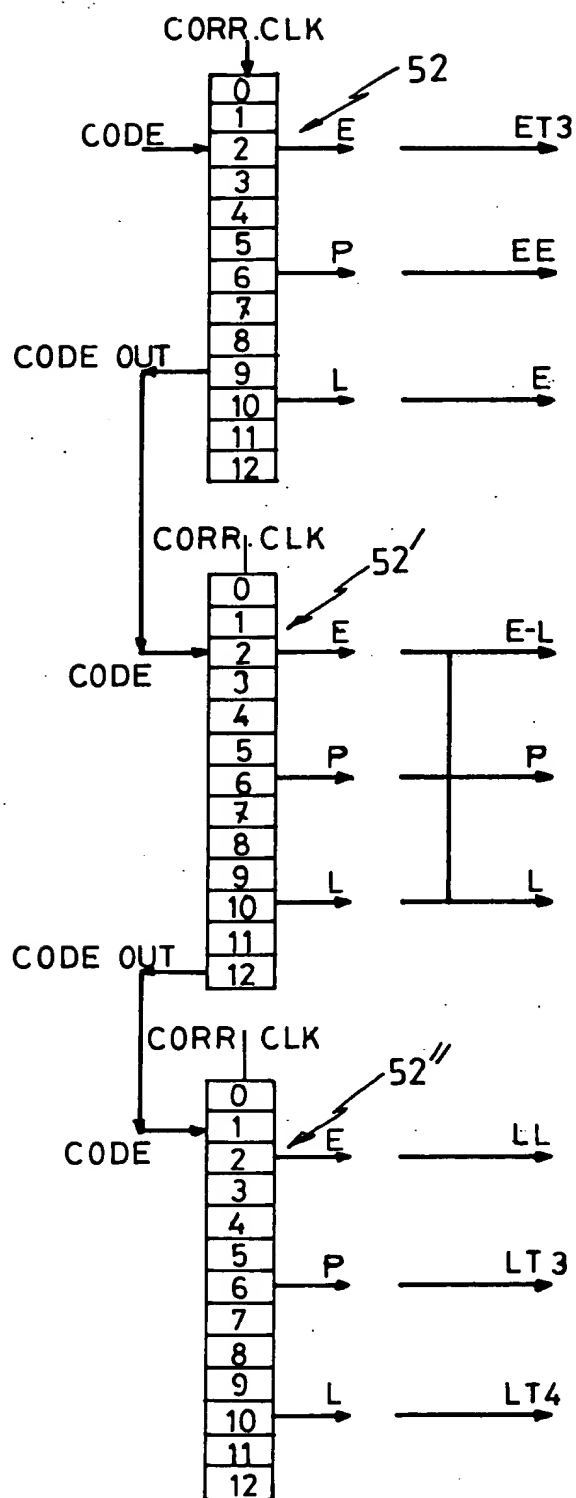
FIG. 8





(a) FAST ACQUISITION MODE

FIG. 9a



(b) MULTIPATH MITIGATION WITH 8T SPACING BETWEEN E AND L

FIG. 9b

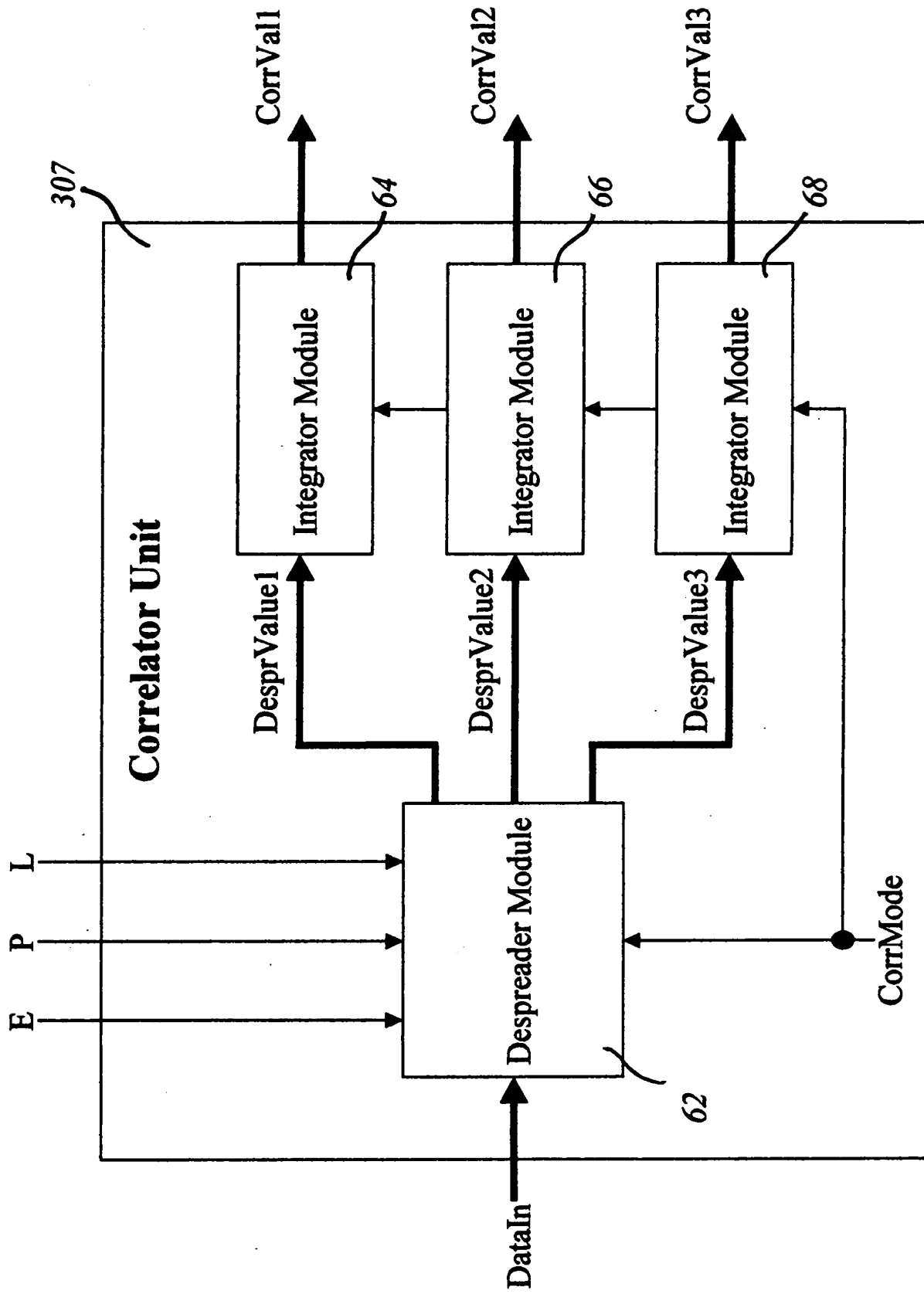


Fig. 10

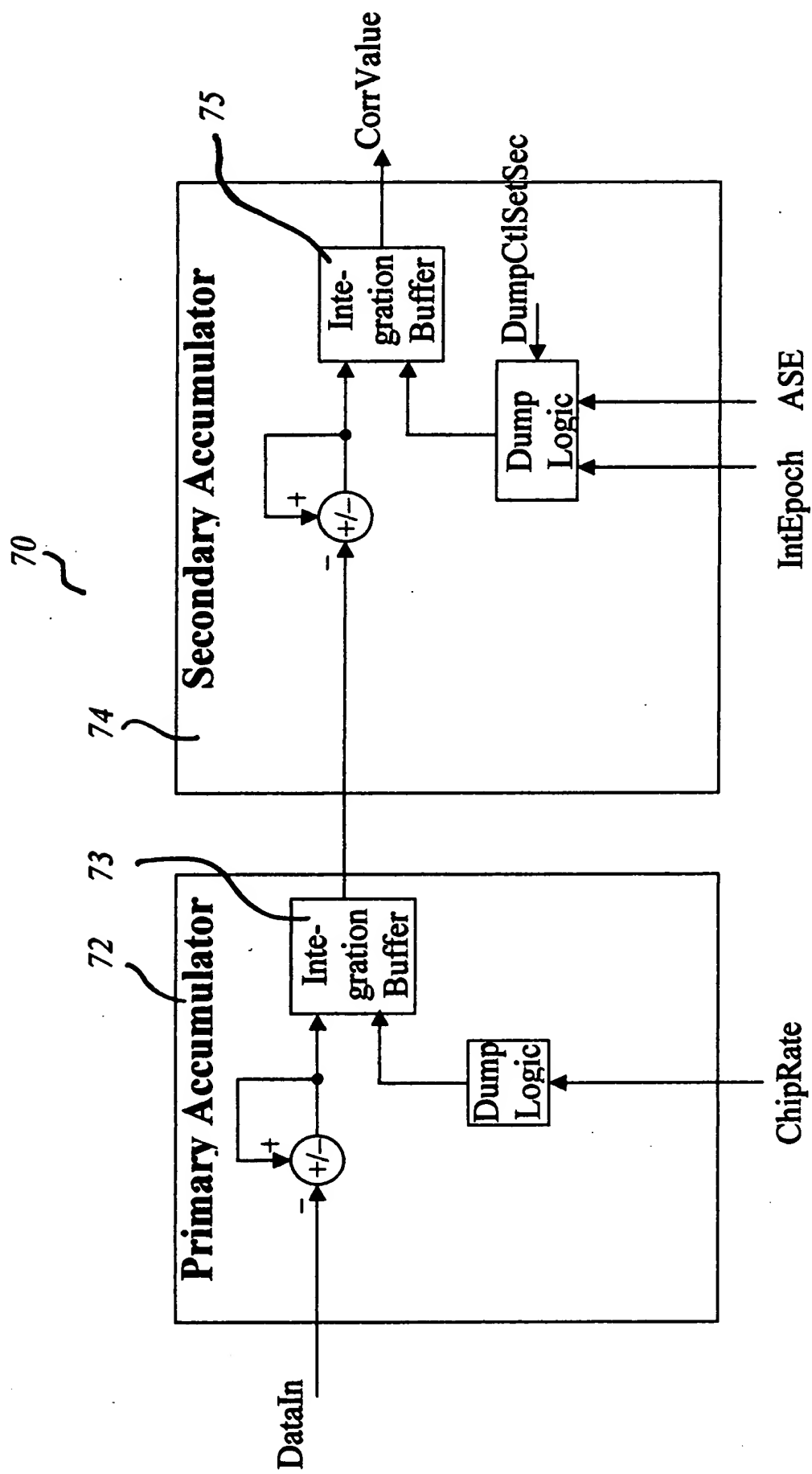


Fig. 11

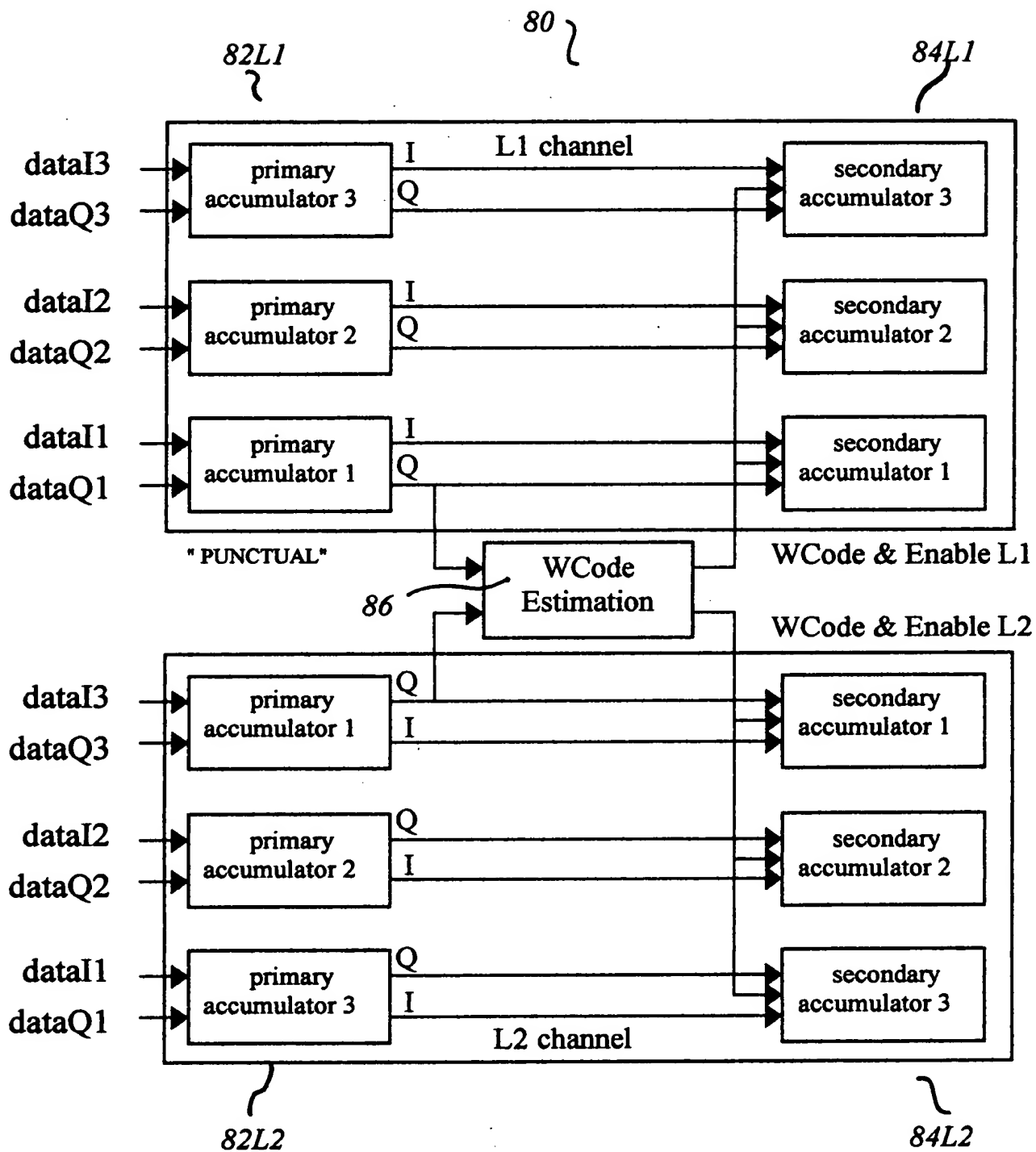


Fig. 13

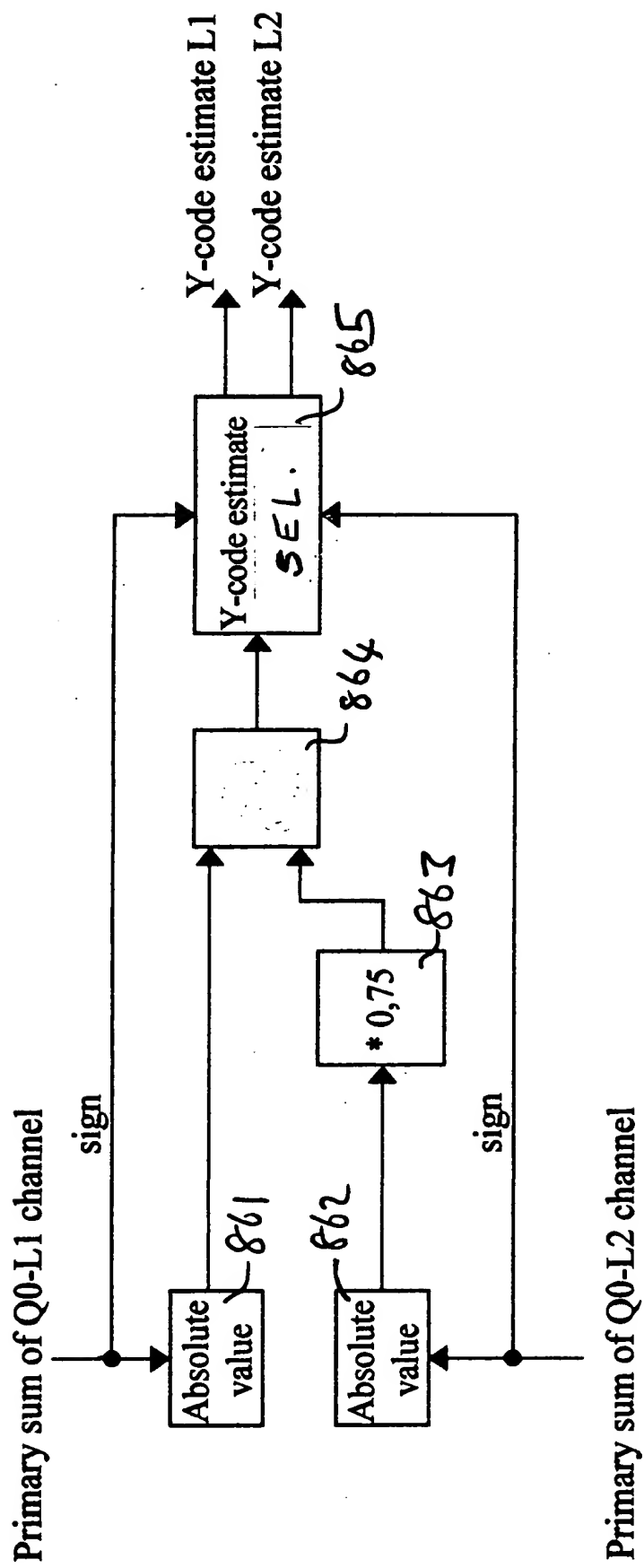


Fig. 14

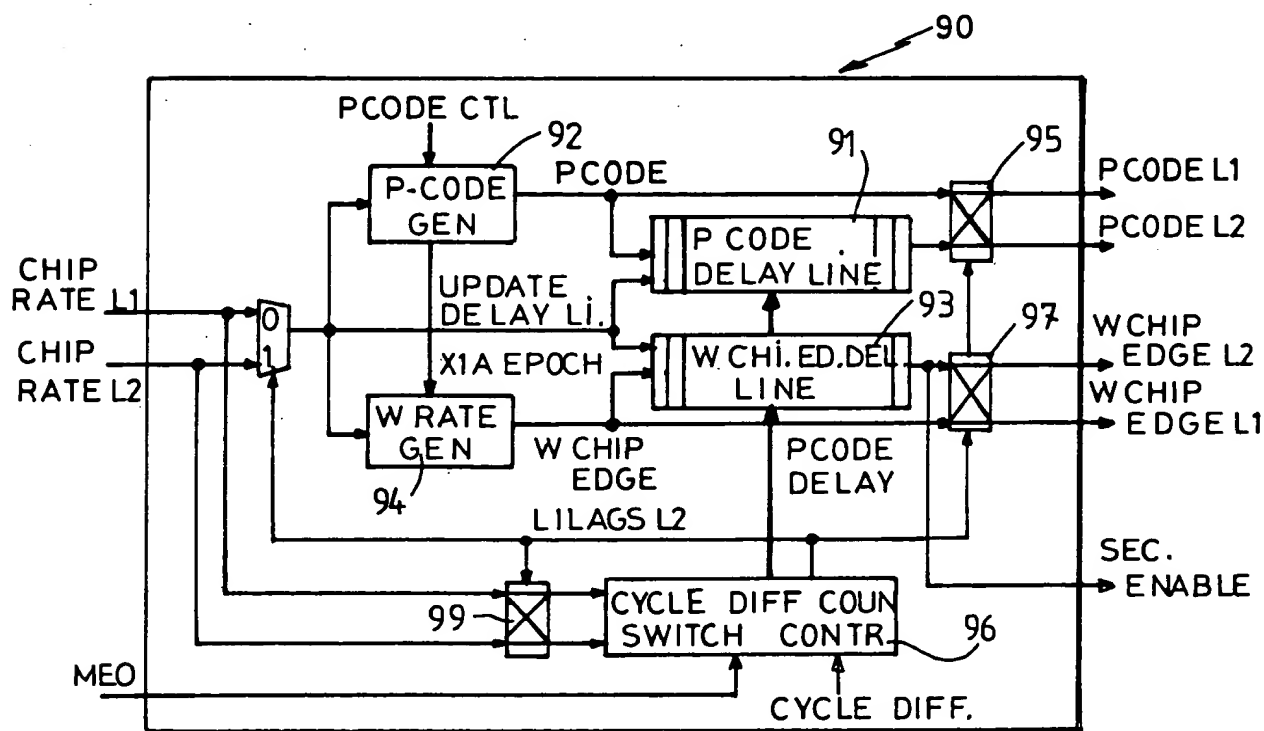
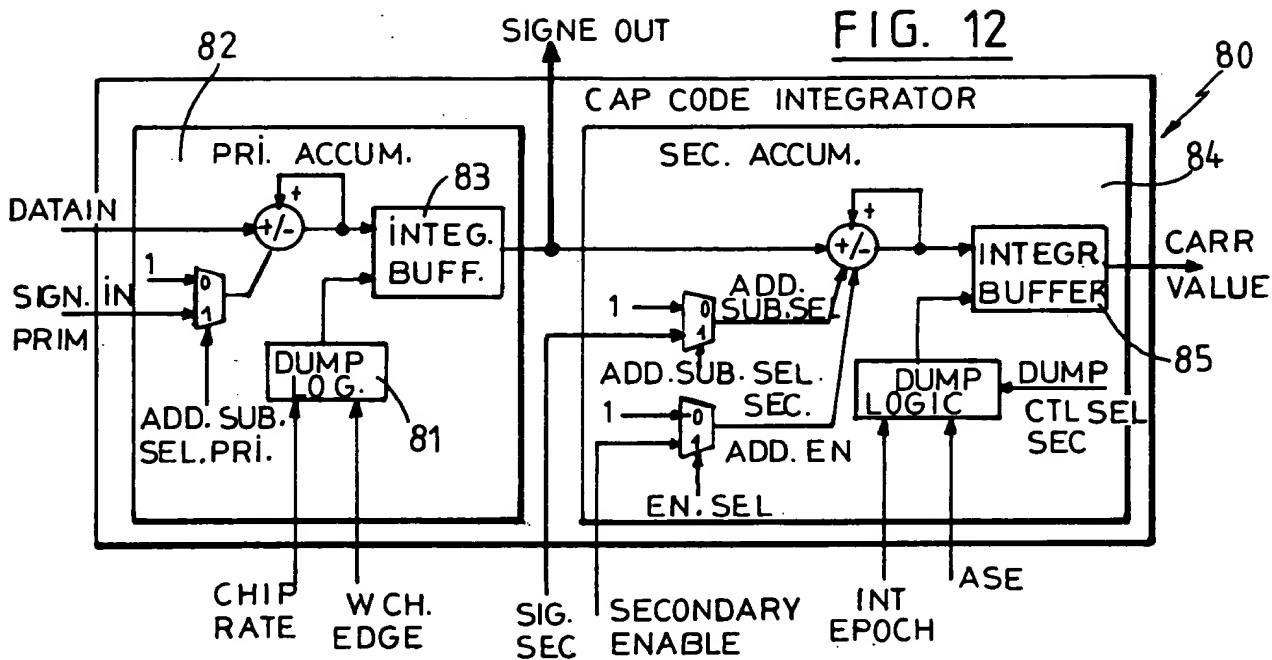


FIG. 15